VLSI Design & Verification - 2 Months
Eligibility – B.E, B.Tech, M.E, M.Tech.

Modules:

- Basic and Advanced Digital Electronics.
- Verilog HDL Design and Verification.
- Introduction to FPGA, FPGA Implementation.
- Communication Protocol Implementation on FPGA.

Platform:

- Lattice Diamond Tool.
- Lattice XO3 eval boards.

Project stream:

- Uart
- Fifo
- SPI

Modules

Section 1 - Recordings		
Basic and Advanced Digital– 3 hrs		
Number System, Logic gates,Boolean Expression, Combinational Circuits	Introduction To Register and Counter (up, down, updown, ring, johnson, ripple counter)	Synchronous Finite State Machine Desig(Mealy and Moore),
Understanding Combinational Logic / Circuit Designing . Canonical Form-SOP, POS	Understanding Sequential logic Circuit/ Circuit Designing Digital design Flow Modeling	Design of basic gates , DFF, TFF using mux,
Section 2- Live Online Sessions		
Digital System Design Using Verilog HDL		
Designing Methodology: Top Down Methodology, Bottom Up Methodology	Verilog data types, Verilog Scalar /Vector, Verilog Arrays, Port declaration	Precedence., Delay concepts
Level of Modeling: Behavioural modeling, data flow modeling, gate level modeling, switch level modeling	Design Simulation and Design Synthesis Methodology of Test Bench.	System task: $monitor, $strobe, $display, $time, $stop, $finsh, $write.
Gate Level Modeling		
Gate Instantiate	Design RTL From logic Diagram	Logic Gate primitive

Delay in Gate level Design	Data Flow modeling ,	Learning about different types of counter, register
Behavioral Modeling		
Structured procedural Statement: Always Statement, Initial Statement ,	Procedural Assignment: Blocking Statement, Non Blocking statement	Timing Control Statement: Delay based timing control, Event Based timing control
Conditional Statement: If..else statement, case statement: casex, casez	Loop: While , do while , for , for each, forever, repeat.	Block statement, Sequential block, parallel Block
Data Flow modeling		
Continuous Assignment statement	Expression, Operator , Operands	Operators: logical, bitwise, reductional, arithmetical, relational , unary, binary, ternary.
Design of Digital Device		
Flip flop (SR, JK, T, D FF), Half adder, Full adder, Ripple carry adder.	Counter (up, down, mod, johnson, ring, ripple, excess-3, gray, load counter)	FSM: Mealy machine, Moore machine. ALU, MAC unit
PWM, CRC, FIFO, Frequency divider program	Shift registers – SISO, SIPO, PISO, PIPO,	Memory Modeling: ROM, RAM
Simulation		
Verilog Simulation basics	Verilog Timescale , Verilog Scheduling region	Verilog Display, task
Project- Digital Clock, Protocol (UART, SPI)		
FPGA Design Basic and Advanced Communication Protocol		
Introduction to FPGA, FPGA Architecture-CLB, I/O block, Interconnetcs	ASIC v/s FPGA v/s CPLD, Types of FPGA, Application of FPGA.	FPGA input/output(IOBS), Special FPGA functions, Logic Synthesis
FPGA Working, Design Flow	H/W Components on FPGA board and their working	Tool Installation : Usage of Diamond tool for FPGA
Implementation of Adder, Subtractor, Counter RAM, ROM, CRC, on Lattice FPGA.	FIFO	Implementation of UART on Lattice FPGA